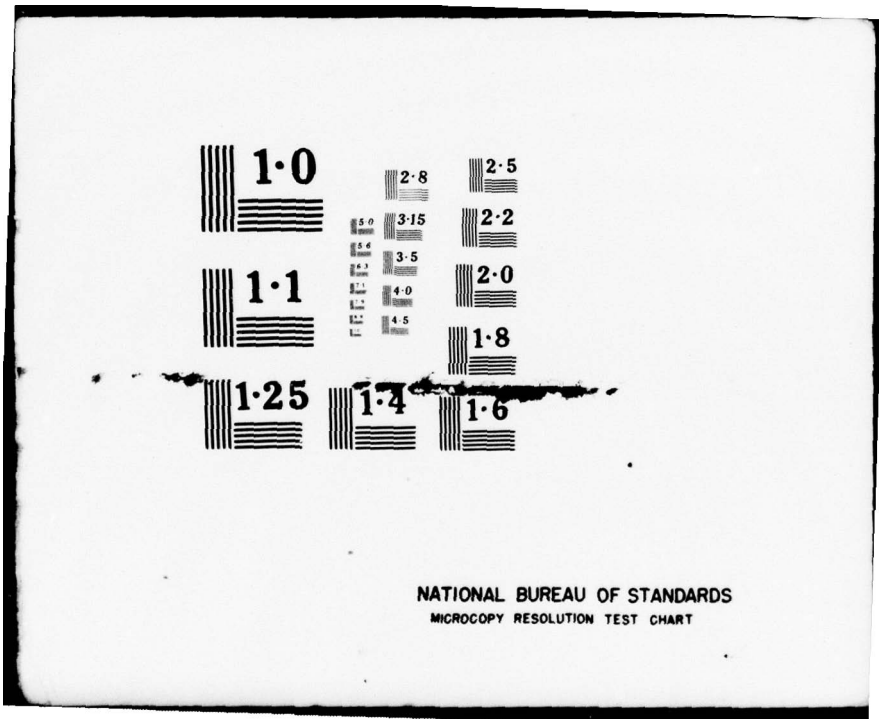
AD-A045 312 ILLINOIS UNIV AT URBANA-CHAMPAIGN DEPT OF COMPUTER SCIENCE F/G 9/2
BLOCK SUM REGISTER AND BURST ARITHMETIC.(U)
AUG 77 J H MA N00014-75-C-0982

UNCLASSIFIED UIUCDCS-R-77-890 NL

| OF |
ADA
045312

END
DATE
FILMED
11-77
DDC


1·0
1·1
1·25
1·4
1·6
1·8
2·0
2·2
2·5
2·8
3·15
3·5
4·0
4·5
5·0
5·6
NATIONAL BUREAU OF STANDARDS
MICROCOPY RESOLUTION TEST CHART

Report No. UIUCDCS-R-77-890 UILU-ENG 77 1746

BLOCK SUM REGISTER AND BURST ARITHMETIC

BY

James Hsioh-Cheng Ma

August, 1977

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

(14) UIUCDCS-R-77-890,
UILU-ENG-77-1746

(6) BLOCK SUM REGISTER AND BURST ARITHMETIC.

BY

(10) JAMES HSIOH-CHENG MA

(9) Master's thesis,

(12) 31p.

(11) August, 1977

(15) N0014-75-C-0982

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1977

ACKNOWLEDGMENT

The author wishes to thank his advisor, Professor W. J. Poppelbaum, for his advice and guidance on the project. He also wishes to thank the members of the Information Engineering Laboratory for their advice and friendship. Special thanks are due to Ehud Bracha for his invaluable aid in the final phase of this project. Finally, the encouragement and support of the author's family has been indispensable and is deeply appreciated.

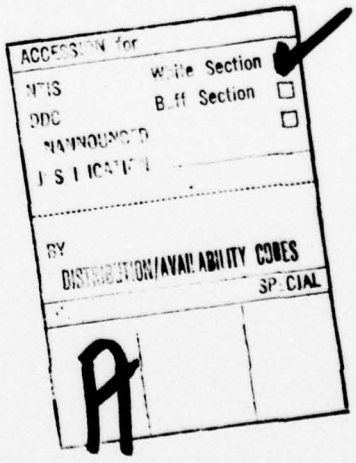


TABLE OF CONTENTS

1. INTRODUCTION

The purpose of this thesis is to develop a simple Block Sum Register and to construct an arithmetic unit capable of addition, subtraction, multiplication, reciprocal, and division using the Block Sum Register.

Burst processing is a method of information representation and processing developed by Dr. W. J. Poppelbaum (1). Burst processing has been shown to be useful for video and audio signal processing. The main idea of burst processing is to represent information by blocks or bursts of unweighed binary digits and to perform simple, low precision processing on these blocks. Figure 1 shows the representation of numbers by a block of length ten. Note that only the number of ones in the block determine the value represented, not the position within the block. Higher precision can be obtained, as shown in Figure 1, if the average of the successive blocks are taken. Therefore, to represent a number to 1% precision, ten bursts of length 10 each will suffice and .1% precision will then require one hundred bursts of length 10 each.

Bursts of length 10 are convenient for decimal arithmetic and will be assumed for the rest of the paper. It is obvious that a single burst can represent eleven numbers from 0 to 1.0 in increments of .1 and thus is capable of approximating a value between 0 and 1.0 to 10% precision. This inherent coarseness of the burst representation results in greatly simplied arithmetic circuitry. The trade off for this simplicity is that burst encoding has lower information capacity than weighed binary: a single burst can represent 11 values, whereas 10 bits of weighed binary can represent 2^{10} values.

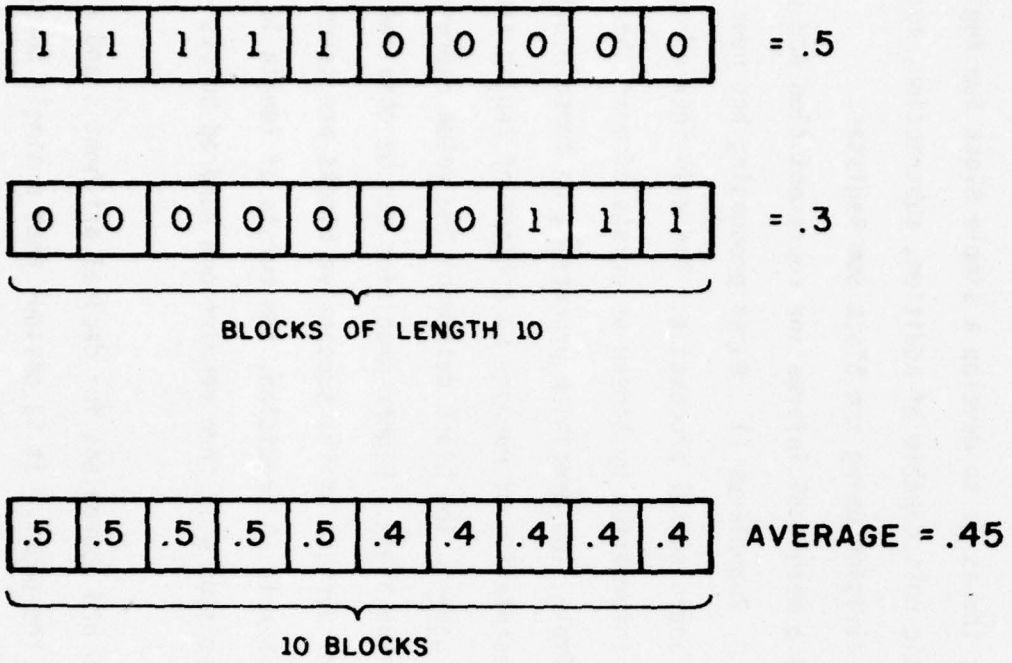


Figure 1. Burst Representation

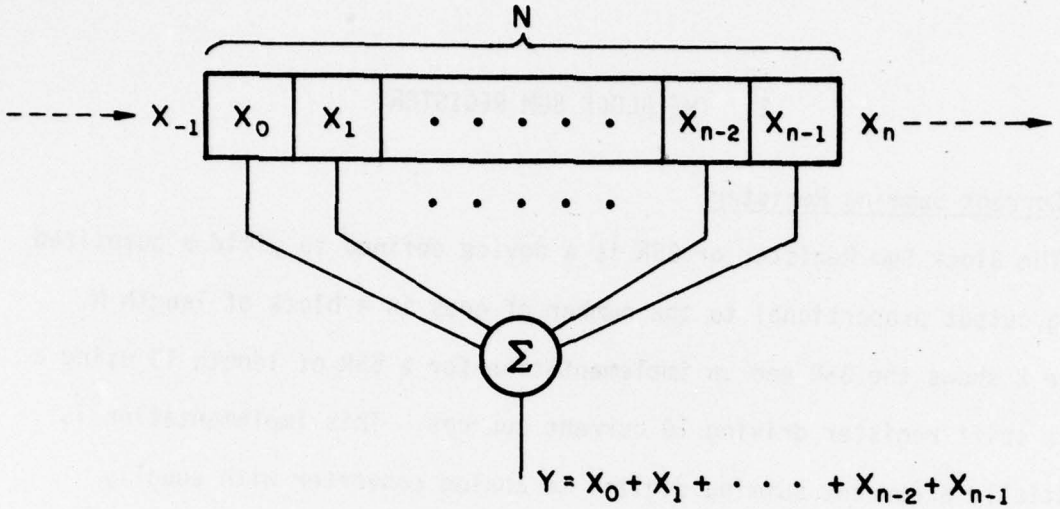
2. THE BLOCK SUM REGISTER

2.1 Current Summing Register

The Block Sum Register or BSR is a device defined to yield a quantized analog output proportional to the number of ones in a block of length N. Figure 2 shows the BSR and an implementation for a BSR of length 10 using a 10 bit shift register driving 10 current sources. This implementation is essentially a current summing digital to analog converter with equally weighted resistors instead of binary multiple resistors. Large output step sizes are possible with this design since the base voltage of each current source is a minimum of 3.5 volts. The burst can also be held in the shift register with the clock stopped without affecting the BSR output. In practice the current sources require close matching of the transistors, which suggest monolithic transistors, and/or variable resistors in order to assure uniform step sizes.

2.2 Charge Summing Register

A different approach to implementing a BSR results in some reduction in complexity and weighted binary output rather than analog output. This would be desirable in interfacing burst and binary processing. Since the number of ones in the shift register can be determined by summing the number of ones entering the shift register and then subtracting the number of ones leaving the shift register, only the first and last bit of the shift register need be examined. Figure 3 shows an implementation based on considering each one to be a unit of charge and using a capacitor to store



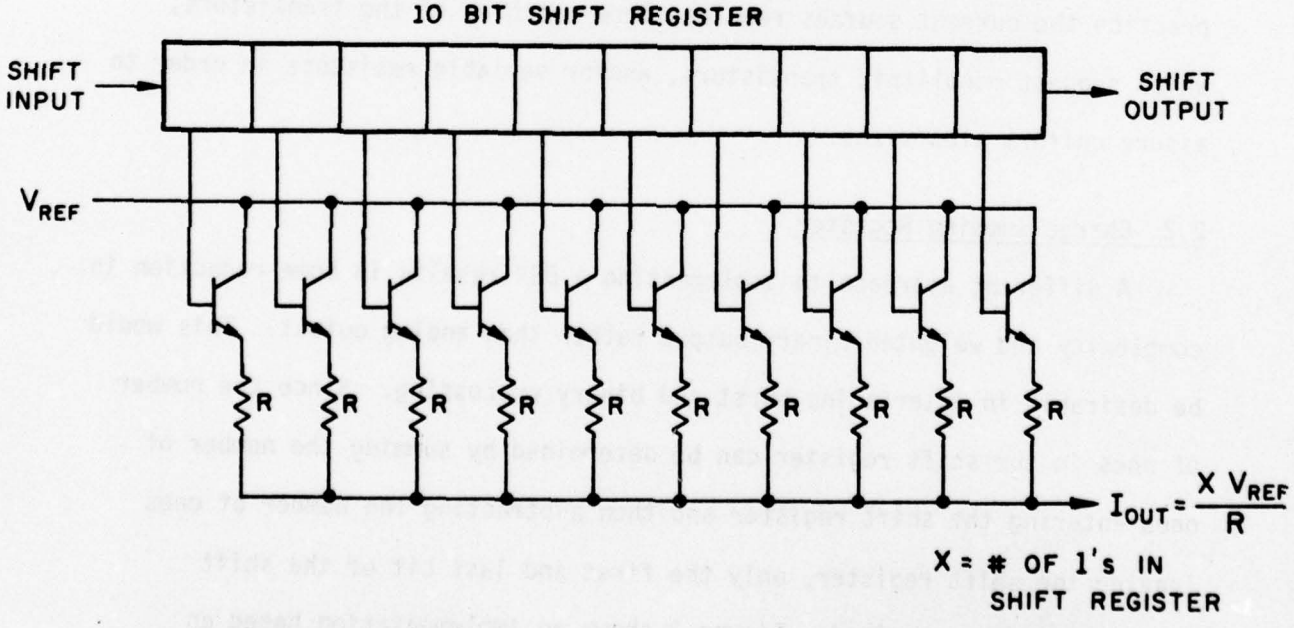


Figure 2. Block Sum Register

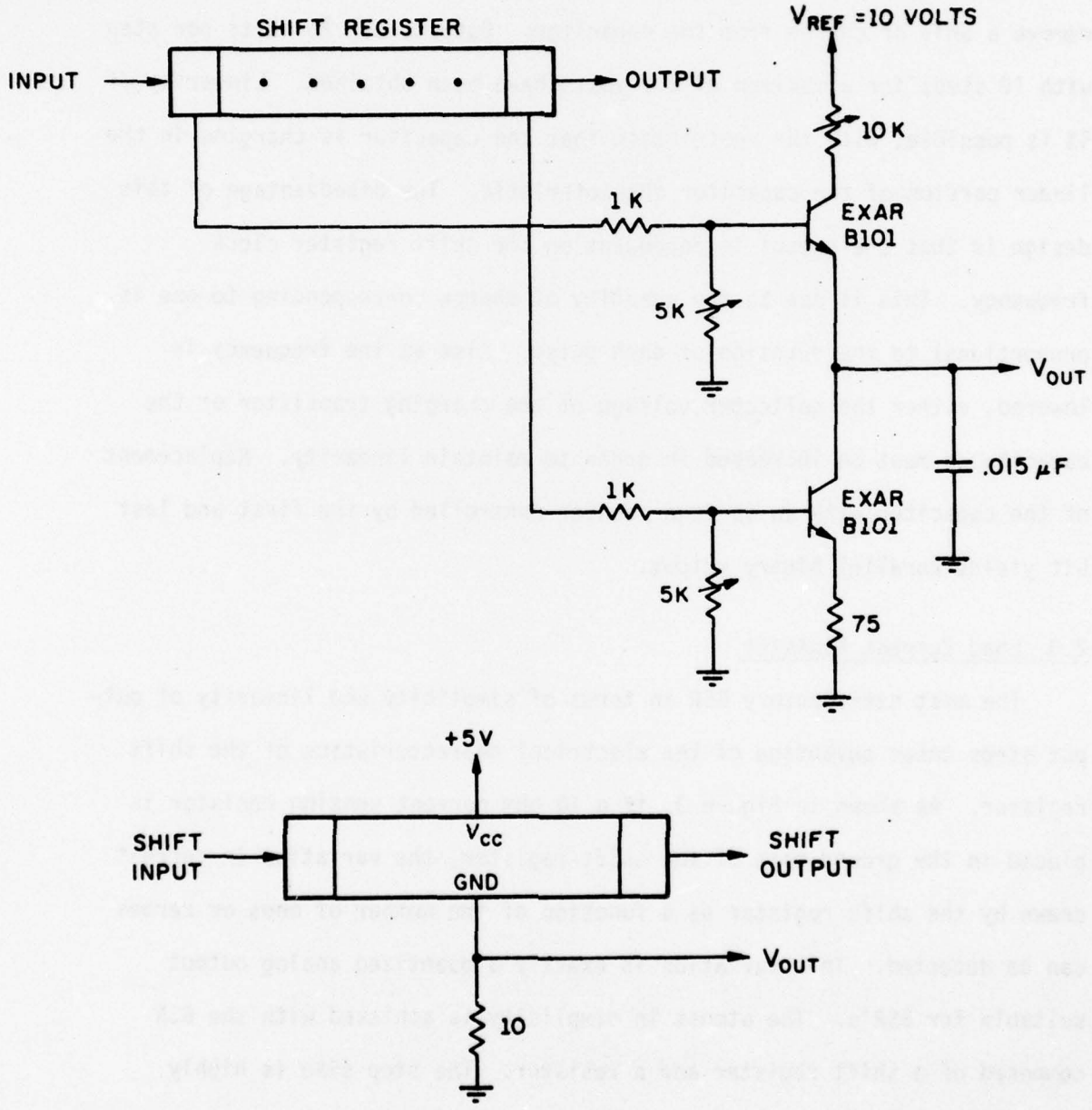
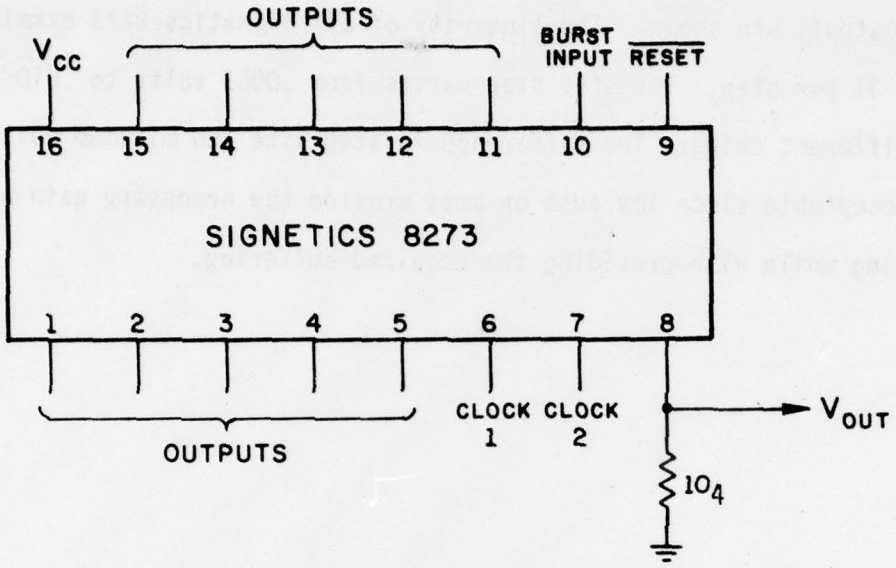


Figure 3. Block Sum Register

these charges. A one entering the shift register would turn on the charging transistor and increment the charge in the capacitor by a unit. A one leaving the shift register would turn on the discharge transistor and remove a unit of charge from the capacitor. Outputs of .25 volts per step with 10 steps for a maximum of 2.5 volts have been obtained. Linearity of 5% is possible, with the restriction that the capacitor is charging in the linear portion of the capacitor characteristic. The disadvantage of this design is that the output is dependent on the shift register clock frequency. This is due to the quantity of charge corresponding to one is proportional to the duration of each pulse. Also as the frequency is lowered, either the collector voltage of the charging transistor or the capacitance must be increased in order to maintain linearity. Replacement of the capacitor with an up-down counter controlled by the first and last bit yields parallel binary output.

2.3 Load Current Register

The most satisfactory BSR in terms of simplicity and linearity of output steps takes advantage of the electrical characteristics of the shift register. As shown in Figure 3, if a 10 ohm current sensing resistor is placed in the ground path of the shift register, the variation in current drawn by the shift register as a function of the number of ones or zeroes can be detected. This variation is exactly a quantized analog output suitable for BSR's. The utmost in simplicity is achieved with the BSR composed of a shift register and a resistor. The step size is highly dependent on the particular shift register used. While all of the 11 shift registers examined showed current variations, only the Signetics 8273 10-bit shift register exhibited sufficient variation in current to be of use.



SIGNETICS 8273 – 10 BIT SERIAL IN PARALLEL OUT SHIFT REGISTER

MINIMUM FREQUENCY – 25 MHz

NUMBER OF ONES	SAMPLE OUTPUT VOLTAGES (±.0002 VOLTS)	
10	.144	.150
9	.153	.159
8	.162	.168
7	.171	.177
6	.180	.186
5	.189	.195
4	.198	.204
3	.207	.213
2	.216	.222
1	.225	.231
0	.234	.240

Figure 4. Signetics 8273 Shift Register BSR

Figure 4 shows the Signetics 8273 used as a BSR and its characteristics. Two sample outputs are shown. The linearity of all Signetics 8273 examined were within 3% per step. The step size varies from .0085 volts to .010 volts for different chips. The difference in step size and minimum voltage level are acceptable since low cost op amps provide the necessary gain and level shifting while also providing the required buffering.

3. A BURST ARITHMETIC UNIT

The use of Block Sum Registers allow on-line arithmetic operations to be performed on burst encoded information in a simple manner with results immediately available in analog or burst format. Since burst representation on a single block basis approximate the information encoded to 10% precision (with higher precision obtained through averaging), the arithmetic circuits can also be of 10% precision. There is difficulty achieving higher precision in multiplication and division, since the average of products and quotients is not the same as products and quotients of the averages. Addition and subtraction does not suffer from this problem. This problem has been considered by Bracha (2) and the results show that with some restrictions on the rate of change of the input sequences of burst operands, the error can be kept to a minimum. The operands in this arithmetic unit are assumed to be positive numbers.

The output of the BSR is either a current or a voltage, so analog arithmetic methods can be applied to burst encoded operands. Analog arithmetic has the advantages of virtually no delay and fairly simple circuits. Up to 1% precision can be obtained. Due to constraints in the multiplier, the analog voltages corresponding to the values of the burst are defined to be negative 1 volt to negative 6 volts, in negative .5 volt decrements, mapped onto burst values of 0 to 1.0 in increments of .1.

3.1 Burst Addition

Addition is performed by summing the voltages of the BSRs containing the burst operands. Figure 5 shows the circuit. The result is scaled to

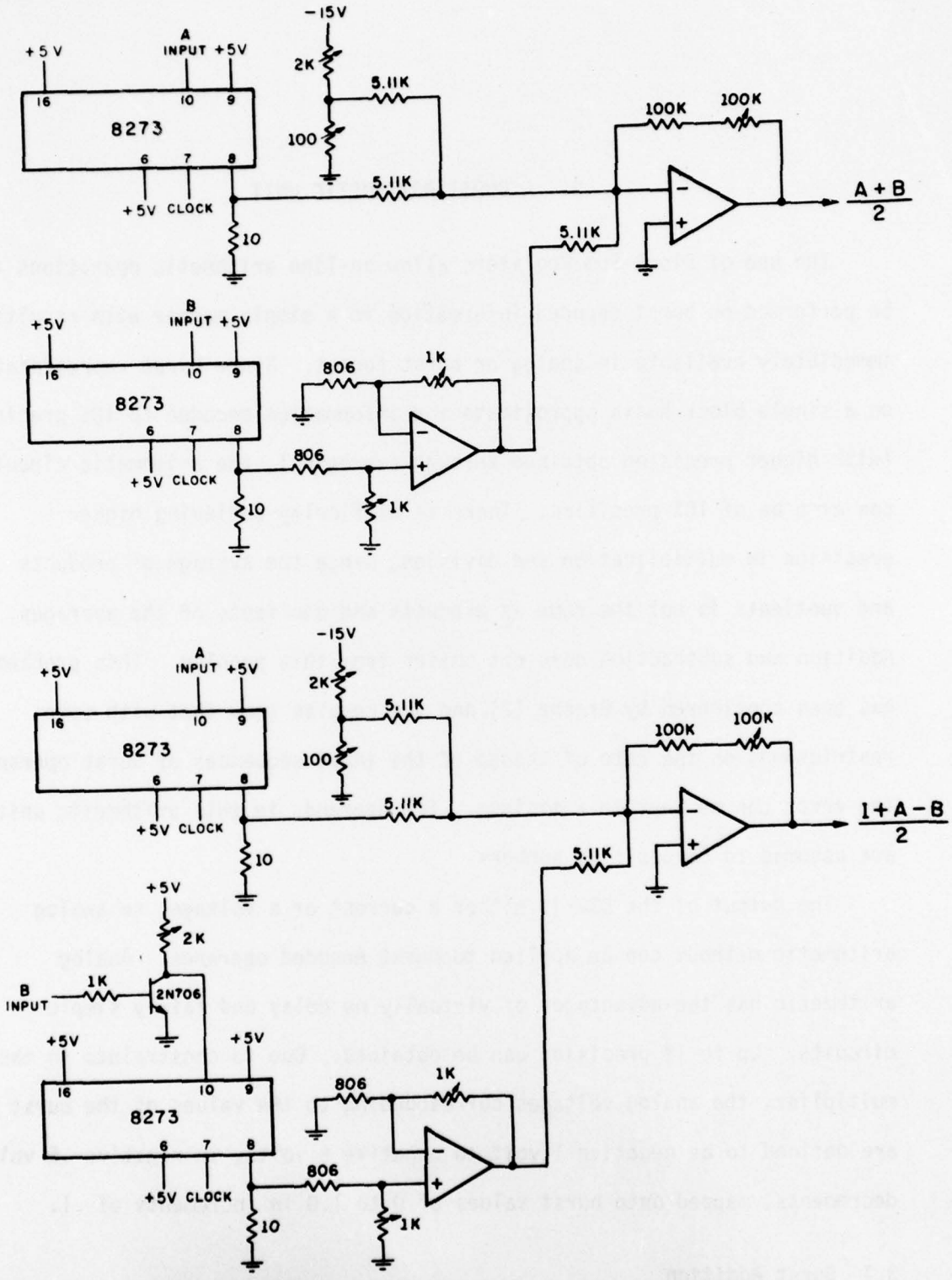


Figure 5. Adder and Subtractor

(A+B)/2 to facilitate encoding into burst format. The main sources of error come from the difference in step sizes, nonlinearity, and difference in DC bias of the BSR outputs. Nonlinearity is less than 3% and adjusting the summing resistors of the amplifier matches the step size and DC bias.

3.2 Burst Subtraction

Subtraction in the form of 1 + A - B can be easily accomplished by complementing the B-burst to obtain 1 - B and then performing addition. Figure 5 shows the circuit. The B-burst is complemented by a transistor connected in the common emitter configuration. Scaling the results to (1+A-B)/2 is done to allow for encoding into bursts. By leaving the result as 1 + A - B, the problem of negative number representation is avoided. However, the constant factor can be easily removed by adding a positive 6 volts to the summing inputs of the amplifier. The analog circuits used can yield bipolar voltages, so negative numbers could be allowed. It is interesting to note that any number of operands can be added or subtracted simulanteously.

3.3 Burst Multiplication

Multiplication is based on the transconductance method (3). This method is the simplest method for multiplication and is based on the transistor's linear relationship between the collector current and the transconductance. The multiplication property can be understood by differentiation, a simplified Ebers and Moll equation for the transistor.

$$I_c = \alpha I_{es}(e^{qV_{be}/kt} - 1)$$

where I_c is the collector current

α is approximately .99

I_{es} is the emitter saturation current

V_{be} is the base-emitter voltage in volts

$kt/q = 25.69$ mV @ 25^oC

$$\frac{dI_c}{dV_{be}} = (q/kt)\ I_c$$

For small variations

$$\frac{\Delta I_c}{\Delta V_{be}} = \frac{q}{kt}\ I_c$$

or

$$\Delta I_c = \frac{q}{kt}\ I_c \Delta V_{be}$$

Therefore by letting the base voltage be one operand and the collector reference voltage be the other operand, the collector current will be proportional to the product of the two operands. Figure 6 shows the transconductance idea implemented with a simple differential amplifier circuit. The emitter voltage is varied rather than the collector voltage. The output is the difference in the two collector currents.

$$I_{c1} - I_{c2} = \frac{q}{kt} \frac{V_B}{5.07k\Omega} 10^{-3} V_A$$

V_B is limited to be .6 volts less than V_A in order to maintain forward bias on the base-to-emitter junction. This restricts V_B to be negative, with a maximum of negative .6 volts if the V_A is positive. The major source of

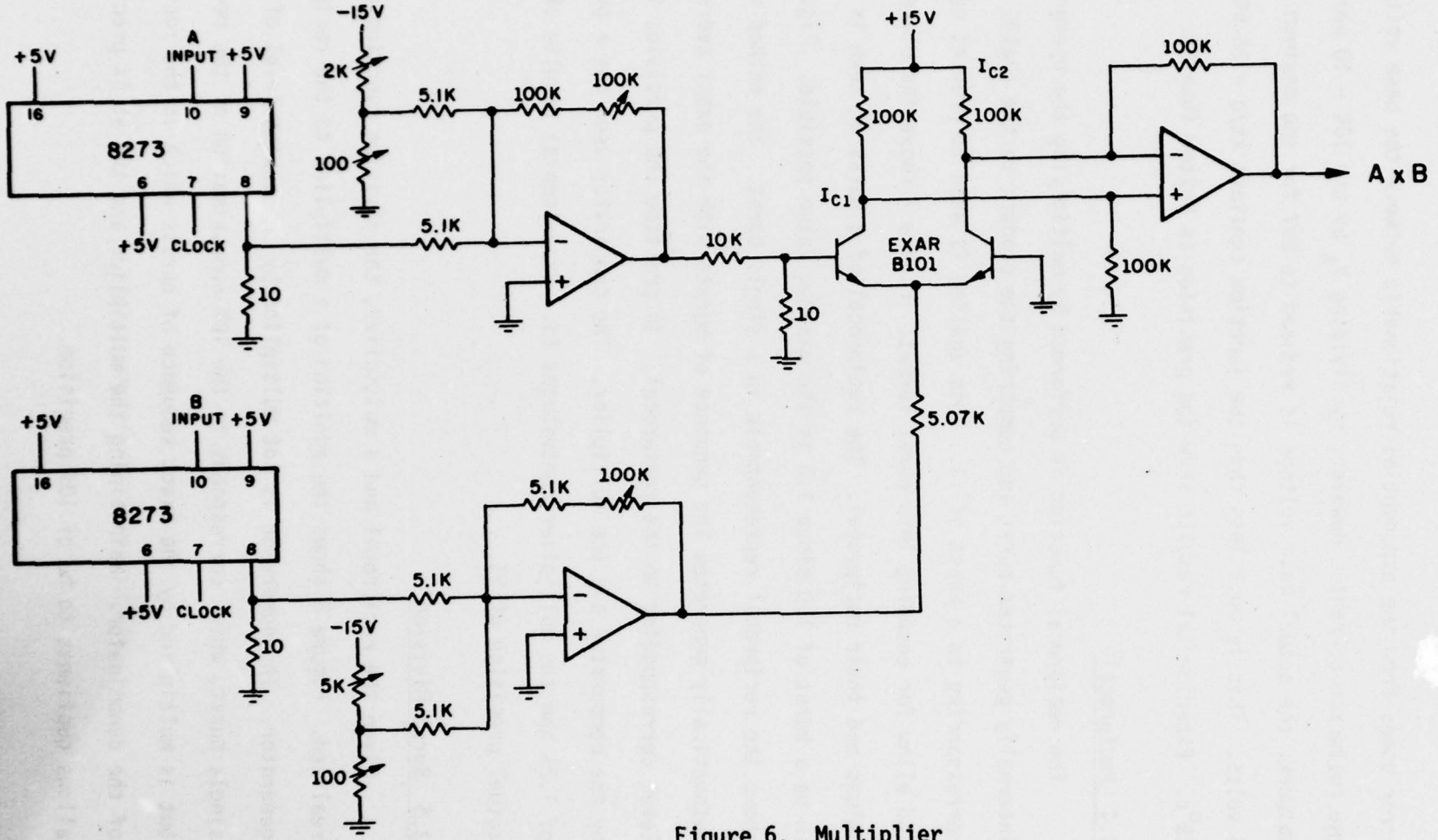


Figure 6. Multiplier

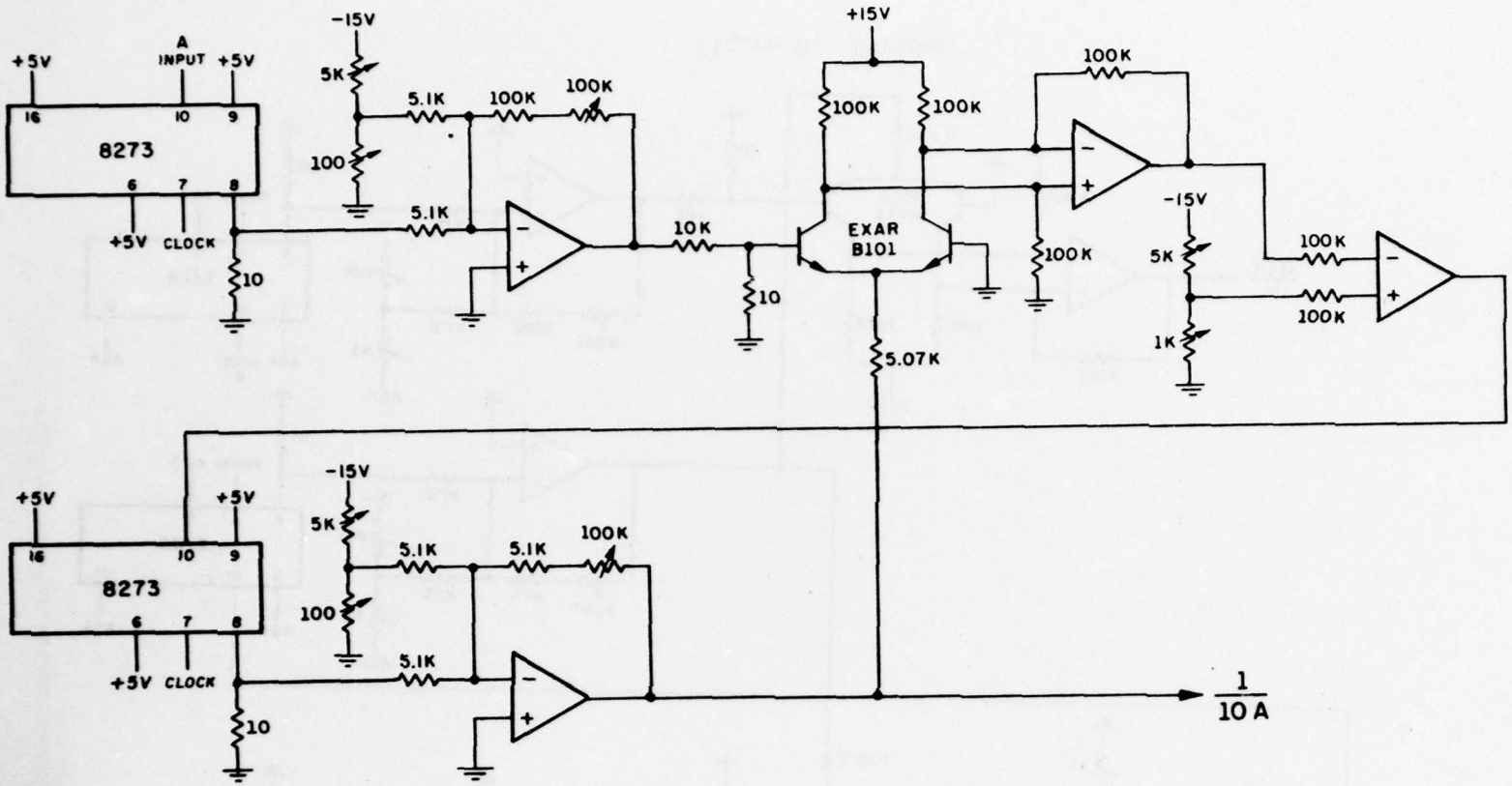
error comes from the exponential relationship between the base voltage and the collector current. However, by dividing V_A by the 10K - 10 ohm divider network, the actual base voltage is reduced to 6mV for the maximum V_A of 6 volts. This is much less than the junction constant kt/q = 25.69 mV at 25^oc. Experimental results show the precision is better than 5%.

3.4 Reciprocal

The reciprocal function is performed by multiplying the operand by an internally generated burst and comparing the product to the analog level corresponding to a burst of .1. This scaling is used to prevent overflow and allow for encoding into burst format. Figure 7 shows the eleven burst values and their reciprocal. The reciprocal of a burst of zero is defined to be a burst of 1.0 since 1.0 is the maximum value possible. Figure 7 also shows the reciprocal representable in a single burst. The method used automatically generates the sequence of bursts with the exact average analog level corresponding to the reciprocal. In practice the precision is limited by the comparator and the multiplier. The comparator used has a precision of 1.2% and the multiplier contributes 5%. Experimental results show actual precision of 5%.

3.5 Burst Division

Given the reciprocal and a multiplier, the division function can be realized. Figure 8 shows the addition of a multiplier to the reciprocal generator. The numerator is not multiplied by the analog level of the single burst, which corresponds to the 10% approximation of the reciprocal, but is multiplied by the exact sequence of bursts which is the reciprocal of the denominator. Maintaining the multiplier and the at 5% precision allows quotients to be of 10% precision.



A	1.0	.9	.8	.7	.6	.5	.4	.3	.2	.1	0
$\frac{1}{10\,A}$	1.0	.111	.125	.142	.166	.2	.25	.333	.5	1.0	1.0
$\frac{1}{10\,A}$ FOR ONE BURST	1.0	.1	.1	.1	.2	.2	.3	.3	.5	1.0	1.0

Figure 7. Reciprocal

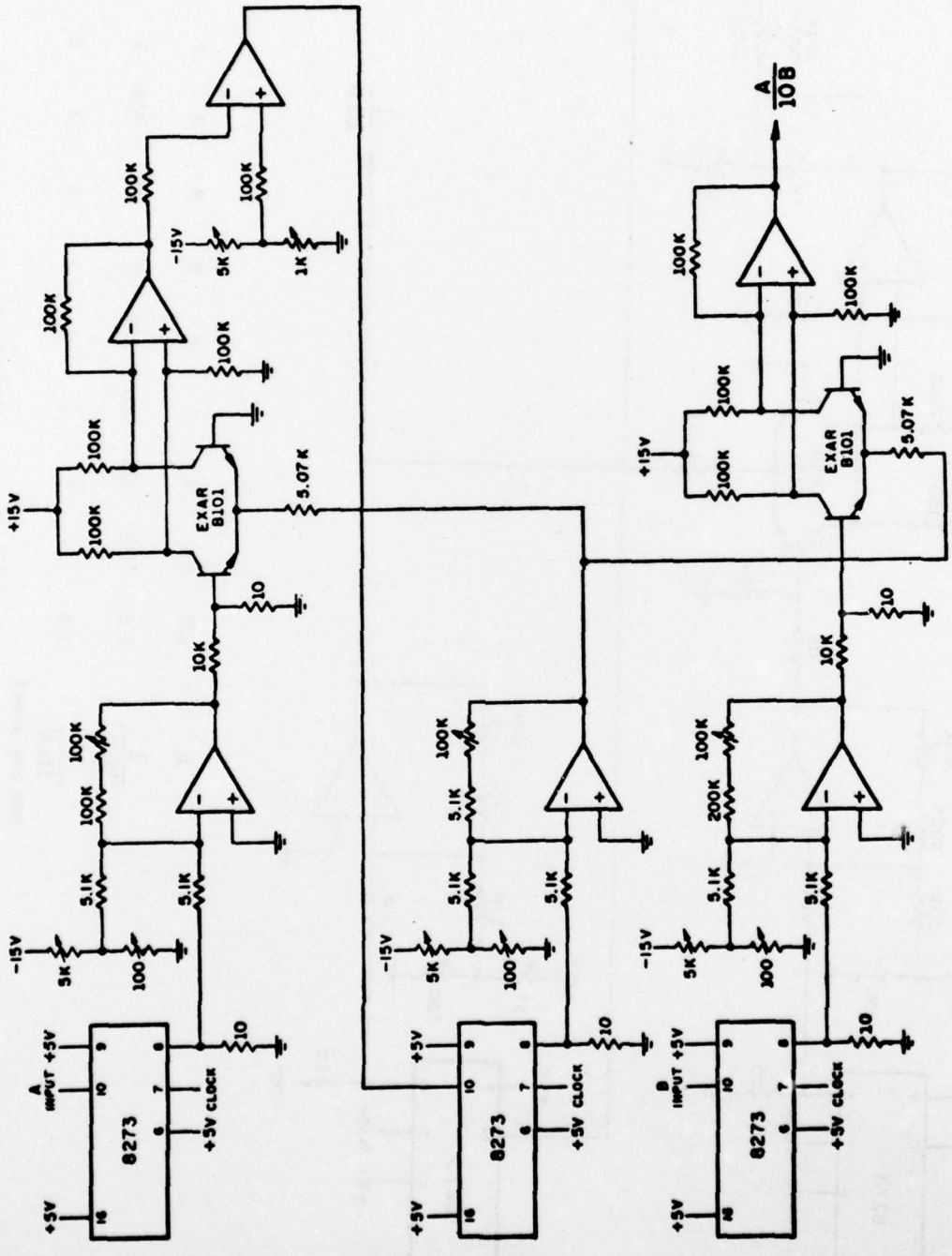


Figure 8. Divider

4. PHYSICAL LAYOUT AND OPERATION OF THE AU

The arithmetic unit contains six banana plugs for +5 volts, ± 15 volts, ground and clock, two sets of ten switches and a banana plug for the output. The arithmetic circuitry has been described and will not be considered here.

Since the load current variation of the Signetics 8273 shift register depends not only on the number of ones in the shift register, but also on whether the clock is high or low, the duty cycle should be 5% or less to minimize the variations in the outputs of the arithmetic circuitry.

The two sets of input switches provide constant bursts to the arithmetic unit. Each switch corresponds to a time slot in the bursts. The switches are inputs to a Signetics 8274 ten bit parallel input shift register. On every tenth clock pulse, the logic levels corresponding to the switch positions are loaded into the Signetics 8274 shift register and shifted out serially during the next ten clock pulses.

The internal outputs of the arithmetic circuits are in analog form. These outputs are encoded into burst format and are available at the output banana plug. The encoding is performed by comparing the analog output with the voltage level corresponding to each burst value. The output of the ten comparators are loaded into a Signetics 8274 shift register on every tenth clock pulse and shifted out during the next ten clock pulses.

The photograph at the end of the Appendix shows the arithmetic unit.

5. CONCLUSIONS

A Block Sum Register composed of one shift register and one resistor has been developed. The BSR developed offers good linearity and ease of use. Depending on the application some form of buffering may be necessary. The buffering amplifier would also provide any needed level shifting or amplification. The BSR is rated at 25 MHz minimum.

A low precision arithmetic unit has also been constructed using the Signetics 8273 shift register as the BSR. The clock frequency of the shift register is 600 KHz, due to the limitation of the 741 op-amp used. The arithmetic unit uses 4 shift registers, 4 transistors, and 7 op-amps. Negative numbers could be allowed since the analog circuitry can yield bipolar voltages. Higher speeds can be obtained by using a faster op-amp or by using a fixed gain discrete amplifier.

Burst representation lends itself to applications where precision is not critical or when it can be obtained through averaging. The simplifications result in low cost precessing elements operating on line. The BSR is a semianalog device performing processing in analog and storage and transmission in digital format.

LIST OF REFERENCES

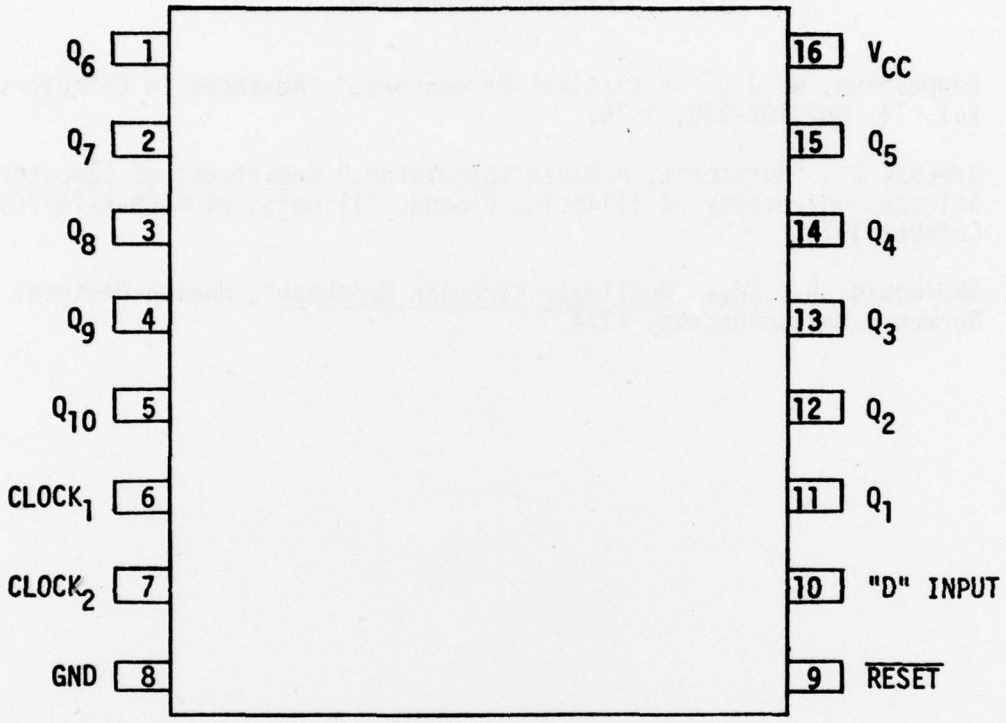
1. Poppelbaum, W. J., "Statistical Processors," "Advances in Computers," Vol. 14, pp. 182-230, 1976.

2. Bracha, E., "Burstcalc, A Burst Calculator," Department of Computer Science, University of Illinois, Urbana, Illinois, UIUCDCS-R-75-769, October 1975.

3. Sheingold, D., ed., "Nonlinear Circuits Handbook", Analog Devices, Norwood, Massachusetts, 1974.

PIN CONFIGURATION

B,F,W Package



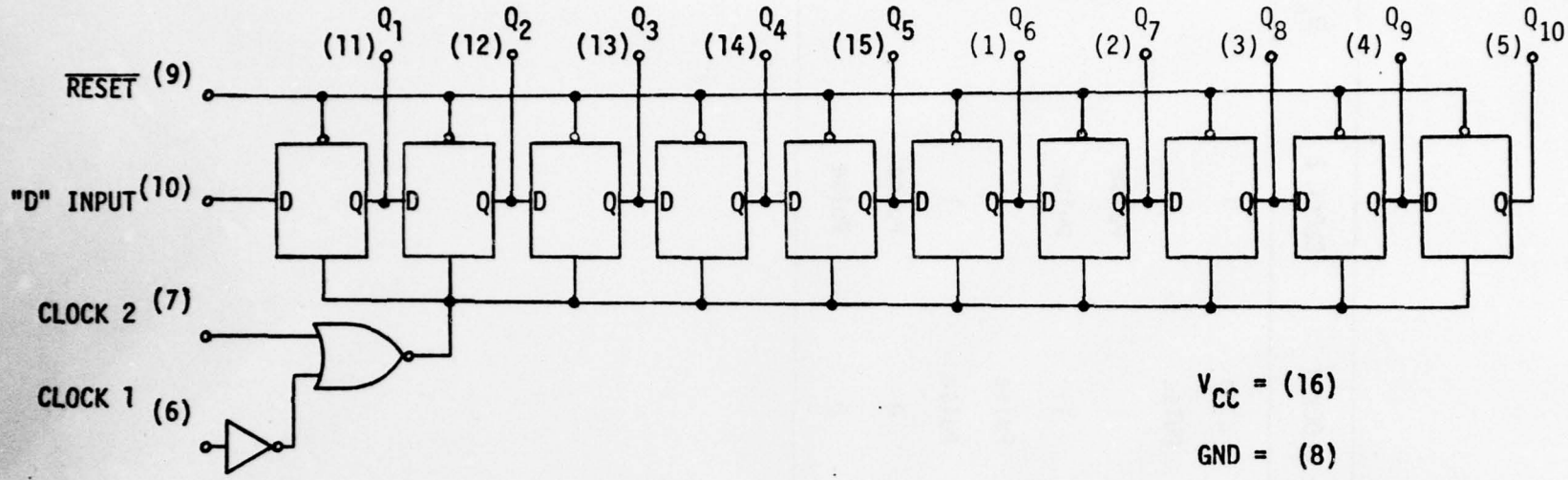
DESCRIPTION

The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

TRUTH TABLE

INPUT	$\overline{\text{RESET}}$	CLOCK 1	CLOCK 2	$Q_n + 1$
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

LOGIC DIAGRAM



V_{CC} = (16)

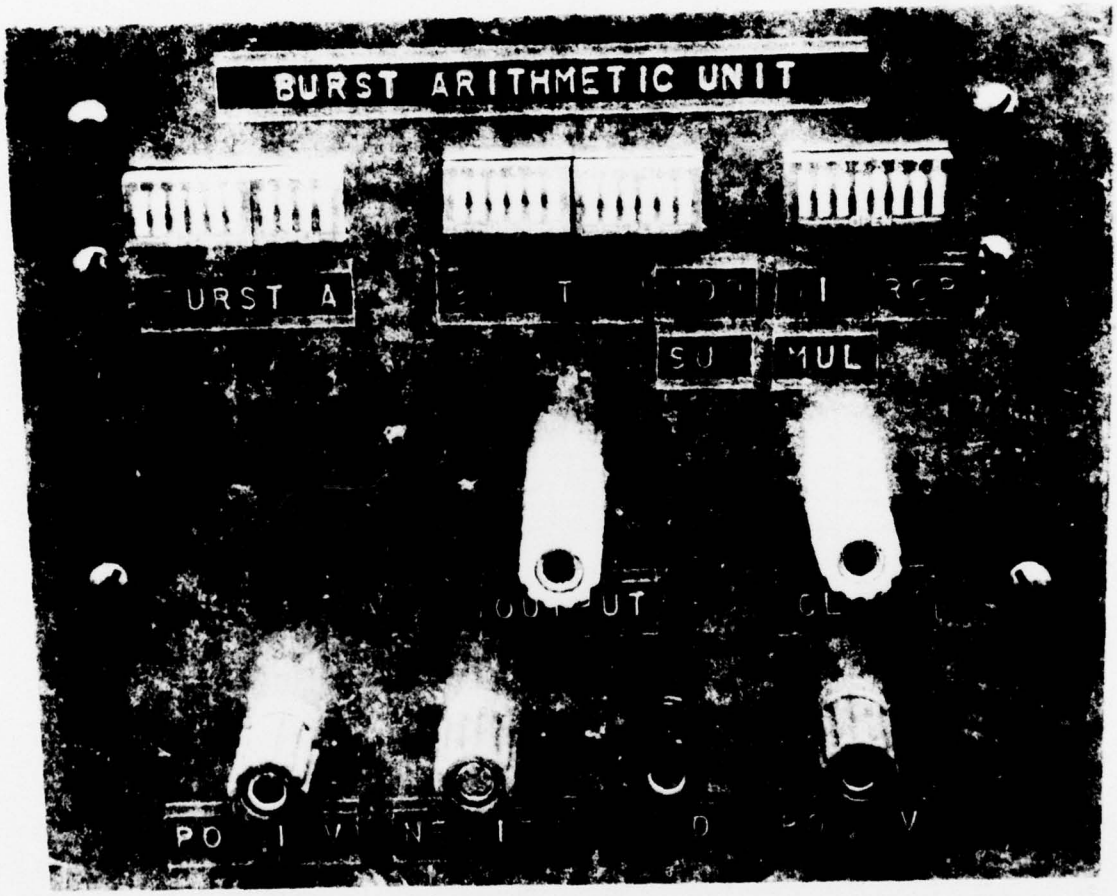
GND = (8)

( ) = denotes pin numbers

10-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

Switching Characteristics $T_A = 25^oC$, $V_{CC} = 5V$

PARAMETER		FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Data Transfer Rate					25	35		MHz
t_{on}	Turn-on delay	Clock 1		Clock 2 = 0V: RESET = 4.5V		32	40	
		Clock 2		RESET = 4.5V		28	40	ns
		Reset		Clock 1 = 4.5V		35	50	
t_{off}	Turn-off delay	Clock 1		Clock 2 = 0V		25	40	ns
		Clock 2		Clock 1 = 4.5V		19	40	
$t_{w(clock)}$	Width of clock Input pulse	Clock 1		Clock 2 = 0V		16	25	ns
		Clock 2		Clock 1 = 4.5V		12	20	
t_{set-up}	Setup time	Clock 1		Clock 2 = 0V			15	ns
		Clock 2		Clock 1 = 4.5V			10	
t_{hold}	Hold time	Clock 1		Clock 2 = 0V			15	ns
		Clock 2		Clock 1 = 4.5V			10	



Photograph of the AU.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: UIUCDCS-R-77-890	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): BLOCK SUM REGISTER AND BURST ARITHMETIC	5. TYPE OF REPORT & PERIOD COVERED: M.S. Thesis/August, 1977
6. PERFORMING ORG. REPORT NUMBER	[redacted]
7. AUTHOR(s): James Hsioh-Cheng Ma	8. CONTRACT OR GRANT NUMBER(s): N00014-75-C-0982
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Department of Computer Science, University of Illinois at Urbana-Champaign, Urbana, IL 61801	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: Office of Naval Research, Code 437, Arlington, Virginia 22217	12. REPORT DATE: August, 1977
	13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report): Release Unlimited
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Burst Processing
Block Sum Register

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Block Sum Register (BSR) is a basic building block used in Burst Processing. The main difficulty with it has been the large number of discrete components required for the current sources.

The paper introduces various BSR designs with considerably smaller numbers of discrete components using the electrical characteristics of the BSR's shift register. The best design is then used in an arithmetic unit which performs

→ next page

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20. the basic arithmetic operations, i.e., addition subtraction, multiplication and division.

BIBLIOGRAPHIC DATA SHEET	1. Report No. UIUCDCS-R-77-890	2.	3. Recipient's Accession No.
4. Title and Subtitle BLOCK SUM REGISTER AND BURST ARITHMETIC			5. Report Date August, 1977 6.
7. Author(s) James Hsioh-Cheng Ma			8. Performing Organization Rept. No. UIUCDCS-R-77-890
9. Performing Organization Name and Address Department of Computer Science University of Illinois at Urbana-Champaign Urbana, IL 61801			10. Project/Task/Work Unit No. 11. Contract/Grant No. N00014-75-C-0982
12. Sponsoring Organization Name and Address Office of Naval Research Code 437 Arlington, Virginia 22217			13. Type of Report & Period Covered Master's Thesis 14.

15. Supplementary Notes

16. Abstracts

The Block Sum Register (BSR) is a basic building block used in Burst Processing. The main difficulty with it has been the large number of discrete components required for the current sources.

The paper introduces various BSR designs with considerably smaller numbers of discrete components using the electrical characteristics of the BSR's shift register. The best design is then used in an arithmetic unit which performs the basic arithmetic operations, i.e., addition, subtraction, multiplication and division.

17. Key Words and Document Analysis. 17a. Descriptors

Burst Processing
Block Sum Register

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

18. Availability Statement	19. Security Class (This Report)	21. No. of Pages
Release Unlimited	UNCLASSIFIED	
	20. Security Class (This Page) UNCLASSIFIED	22. Price